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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/814,321	03/21/2001	Gary F. Feierbach	ALP1P203	4455

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EXAMINER	
CHEN, TSE W	

ART UNIT	PAPER NUMBER
2116	

DATE MAILED: 05/02/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/814,321	FEIERBACH, GARY F.	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-8,17-25 and 39* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *17-25* is/are allowed.

6)☒ Claim(s) *1-8 and 39* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. It is hereby acknowledged that the following papers have been received and placed of record in the file: Amendment dated March 14, 2006.

2. Claims 1-8, 17-25 and 39 are presented for examination.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bartley, U.S. Patent 6219796, in view of Fletcher et al., U.S. Patent 6611920, hereinafter Fletcher.

5. In re claim 1, Bartley discloses a method for operating a microprocessor [10] to reduce power consumption [abstract], the microprocessor including a functional unit [11] formed of a plurality of stages [functional units] [col.3, ll.1-30, ll.41-65], the method comprising:

- Evaluating instructions to be executed to determine the operation type of each of said instructions, the instructions to be executed depending on operation type by said plurality of stages of said functional unit [col.4, ll.54-57; col.5, ll.1-15, ll.33-44, ll.51-57].
- Producing activity indicators [bit level machine code of either sleep or active implicit restoration instructions] by reading an operation type from an instruction and providing an associated signal [bit level machine code of either sleep or active implicit restoration instructions] based upon the operation types of said instructions [col.4, ll.54-57; col.5, ll.1-2, ll.33-44, ll.51-57; col.6, ll.8-18].

- Following said steps of evaluating said instructions and producing said activity indicators, controlling the supply of current to each of said plurality of stages such that only selected stages of said plurality of stages will draw current from a power supply, the controlling being based upon activity indicators associated with each of said stages [col.6, ll.33-52; powering down is done after evaluating and producing steps].
- Advancing said instructions with the microprocessor [col.3, ll.16-30; operations advanced serially in stages].
- Executing said instructions that are within each of said selected stages [col.3, ll.52-61].

6. Bartley did not disclose explicitly that the stages are arranged in series or discuss the details of controlling the supply of current.

7. Fletcher discloses a method for operating a microprocessor [integrated circuit] to reduce power consumption [abstract], the microprocessor including a functional unit [FUB logic 310] formed of a plurality of stages [logical stages 310.1-310.N], where said stages of said functional unit are arranged in series [pipeline], the method comprising:

- Producing activity indicators [enable, disable] by reading an operation type from an instruction [instruction itself indicates operation type to determine enabling/disabling of clock] and providing an associated signal comprising one of a clock marker [enable] or a no-clock marker [disable] based upon the operation types of said instructions [col.3, ll.53-67].
- Following a step of producing activity indicators, controlling the supply of current to each of said plurality of stages by providing a clock signal [primary clock] and the activity indicators to a logic gate [330] that determines that only selected stages of said

plurality of stages will draw current from a power supply, the controlling being based upon activity indicators associated with each of said stages [col.3, ll.53-67; col.4, ll.1-14, ll.27-30; clock and activity indicators from scheduler control current draw following the production of activity indicators].

- Advancing the instructions within said microprocessor [col.3, ll.53-67; col.4, l.61 -- col.5, l.5].
- Executing said instructions that are within each of said selected stages [col.4, ll.27-37].

8. It would have been obvious to one of ordinary skill in the art, having the teachings of Bartley and Fletcher before him at the time the invention was made, to modify the microprocessor as taught by Bartley to include the functional unit as taught by Fletcher, in order to obtain the functional unit having the plurality of independently controlled stages arranged in series, as the pipeline series arrangement of stages is a very well known arrangement suitable for use with the microprocessor of Bartley; and providing the associated signal comprising one of a clock marker or a no-clock marker based upon the operation types of the instructions, as the utilization of clock to control the supply of current is a very well known concept suitable for use with the microprocessor of Bartley. One of ordinary skill in the art would have been motivated to make such a combination as it increases processing efficiency [via pipeline arrangement] and provides a refined way [via clock control] to decrease power consumption in a processor as the processing power increases and potential overheating is a problem [Fletcher: col.1, ll.13-32].

9. As to claim 2, Bartley discloses the microprocessor that is a very long instruction word processor [col.3, ll.41-44].

10. As to claim 3, Bartley discloses the evaluating operates to determine whether each of said instructions is an operation instruction type [active] or a no-operation instruction type [sleep] [col.5, l.51 - col.6, l.7].

11. As to claim 4, Fletcher discloses the type of instructions executed in each of said selected stages is an operation instruction type [col.4, ll.27-60].

12. As to claim 5, Bartley discloses the producing operates to produce a power-on activity indicator associated with operation instruction types [implicit], and a power-off activity indicator associated with no-operation instruction types [explicit] [col.5, l.51 - col.6, l.18].

13. As to claim 6, Fletcher discloses the selected stages are associated with power-on activity indicators, and wherein the remaining stages are associated with power-off activity indicators [col.4, l.61 -- col.5, l.13].

14. As to claim 7, Fletcher discloses the controlling operation further comprises transmitting a clock signal only to the selected stages of the functional unit [col.4, ll.10-14].

15. As to claim 8, Fletcher discloses the method further comprising repeating all of the steps for successive instructions [fig.3; pipeline architecture repeats for all instructions].

16. Claim 39 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bartley and Fletcher as applied to claim 1 above, and further in view of Simonvich et al., US Patent 6308241, hereinafter Simonvich.

17. Fletcher discloses the evaluation and producing steps are performed by an instruction evaluation unit [scheduler; col.3, ll.53-67]. Fletcher and Bartley did not discuss the details of an instruction register.

18. Simonvich discloses a method comprising:

- Receiving instructions at an instruction evaluation unit [instruction cache control 118] from an instruction register [cache 114; fig.1; col.3, ll.19-23].
- Receiving instructions at a functional unit [multiplexer 128 and execution 112] from the instruction register [fig.1].

19. It would have been obvious to one with ordinary skill in the art, having the teachings of Simonvich and Fletcher before him at the time the invention was made, to modify the microprocessor as taught by Fletcher to include the configuration with the instruction evaluation and functional units receiving instructions from the instruction register as taught by Simonvich, in order to obtain more efficient processing [Simonvich: col.2, ll.24-47]. One of ordinary skill in the art would have been motivated to make such a combination as it provides a way to reduce power consumption [reduced execution cycle saves power].

Allowable Subject Matter

20. Claims 17-25 are allowed.

Response to Arguments

21. Applicant's arguments filed March 14, 2006 have been fully considered but they are not persuasive. Applicant stipulates that "the functional blocks of the present invention are akin to the blocks L1... of Bartley... the claimed invention operates at a more granular level". Examiner submits that the functional unit and associated stages disclosed by Bartley reads on the claim in relation to both structure and functionality. Absent further limitations that would distinguish the claimed invention at a "more granular level", Examiner respectfully maintains the rejections.

Conclusion

22. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (571) 272-3672. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne Browne can be reached on (571) 272-3670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
March 23, 2006

THUAN N. DU
PRIMARY EXAMINER